REMARKS

Reconsideration and allowance of the subject application are respectfully requested.

Claims 1-30 are pending.

Claims 3, 6, 11, 17, 21, 26 and 29 stand rejected under 35 U.S.C. §112, second paragraph. Applicant respectfully traverses this rejection.

The Examiner indicates that the Applicant does not teach the type of the first and second lines. While Applicant disagrees with the Examiner's assertion, Applicant has amended the claims to recite first data lines instead of data lines of a first type and second data lines instead of data lines of second type.

The Examiner also states that he does not understand the meaning of the term "load" as used in the claims. Applicant believes the use of this term is also quite clear. The Examiner is referred to page 5, line 17 - page 6, line 1, which explains the use of this term with respect to the present invention. Applicant also points out that this explanation is repeated several times in the application.

In view of the above, Applicant respectfully request that the Examiner withdraw this rejection.

Applicant notes with appreciation the Examiner's indication that claims 4, 7, 12-14, 18-19, 22-24 and 27 would be allowed if placed in independent form. At this time, these claims have not been amended into independent form

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because the independent claims from which they depend are believed allowable.

Claims 1-2, 5, 10, 15-16, 20, 25 and 28 stand rejected under 35 U.S.C. §102(e) as being anticipated by Lim. Applicant respectfully traverses this art grounds of rejection.

As an initial matter, Applicant is confused by the rejection of claims 5, 10, 15, 16, 20 and 25. These claims depend from one of claims 4 and 14, which the Examiner has indicated are allowable. Therefore, these dependent claims must be allowable.

Lim discloses a bit line amplifying unit 130 (i.e., a bit line amplifier) that amplifies data on bit lines BL and BLB. A current sense amplifier 110 senses and amplifies data received on a pair of differential input lines IN and INB connected to the output of the bit line sense amplifier 130. A voltage sense amplifier 120 (called a batch amplifying unit) senses and amplifies a voltage level difference of data output from the current sense amplifying unit 110 (see column 2, line 63 - column 3, line 10).

In his art grounds of rejection, the Examiner indicates that bit lines BL and BLB are a bit line sense amplifier. This is simply incorrect. Column 6, lines 5-10 of Lim clearly state that BL and BLB represent bit lines. Instead, the bit line sense amplifier is the bit line amplifying unit 130. Accordingly, Fig. 1 of Lim illustrates a single data sense amplifier formed of a current sense amplifier 110 and a voltage sense amplifier 120 connected to a single bit line amplifier 130. As such, Lim does not disclose or suggest the two different data sense

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amplifiers associated with bit line amplifiers as recited in claim 1 or the two different data sense amplifiers as recited in claim 28.

Claims 1 and 28 are not anticipated or rendered obvious to one skilled in the art by Lim. Therefore, the claims dependent thereon are allowable at least for the reasons stated above with respect to claims 1 and 14.

Applicant respectfully requests that the Examiner withdraw this art grounds of rejection.

New claim 30 includes similar limitations to those discussed above with respect to claim 1 and is also considered allowable.

CONCLUSION

In view of above remarks, reconsideration of the outstanding rejection and allowance of the pending claims is respectfully requested.

If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at number listed below.

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If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

Very truly yours,

HARNESS, DICKEY & PIERCE, PLC

By

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GDY:jcp

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